What is Claimed is:

1. A method of forming a metal line of a semiconductor device, comprising the steps of:

(a) preparing a semiconductor substrate comprising an underlying element and forming an interlayer insulating film thereon;

(b) forming a metal line contact hole to expose a portion of the underlying element, and a metal fuse contact hole to expose a portion of the semiconductor device by etching a portion of the interlayer insulating film;

(c) forming a metal line plug and a metal fuse plug by filling the metal line contact hole and the metal fuse contact hole with conductive materials, respectively;

(d) forming a metal layer on the interlayer insulating film including the metal line plug and the metal fuse plug;

(e) etching the metal layer to form a metal line pattern and a metal fuse pattern electrically connected to the metal line pattern; and

(f) forming the metal line by electrically isolating the metal line pattern and the metal fuse pattern by means of the over-etching process to the metal fuse.

2. The method of claim 1, wherein the metal line pattern is connected to the underlying element through the metal line plug.

3. The method of claim 1, wherein the metal fuse pattern is connected to the semiconductor substrate through the metal fuse plug.

4. The method of claim 1, wherein a space between the metal line pattern and the metal fuse pattern is set to have a width such that the metal layer remains to a constant thickness in the space due to an etching loading effect, even after carrying out the over-etching process of forming the metal line.

5. The method of claim 1, wherein the metal fuse pattern comprises a plurality of condensed patterns, and spaces between the condensed patterns are set to have widths such that the metal layer has a constant thickness in the spaces due to an etch loading effect, even after carrying out the over-etching process of forming the metal line.

6. The method of claim 1, wherein the etching step (e) is performed by an etch process and over-etch process.